

FIG. 1

FIG. 1 is a schematic diagram of a semiconductor device 10. The device is divided into two main regions, 10X and 10Y, by a central vertical line. Region 10X (left) contains a series of horizontal bars 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100. Region 10Y (right) contains a series of horizontal bars 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100. The device includes various components labeled 1 through 10, 15, 16, 5a, 5b, 5c, 6a, 6b, 10X, and 10Y. A coordinate system (X, Y) is shown in the top right corner.

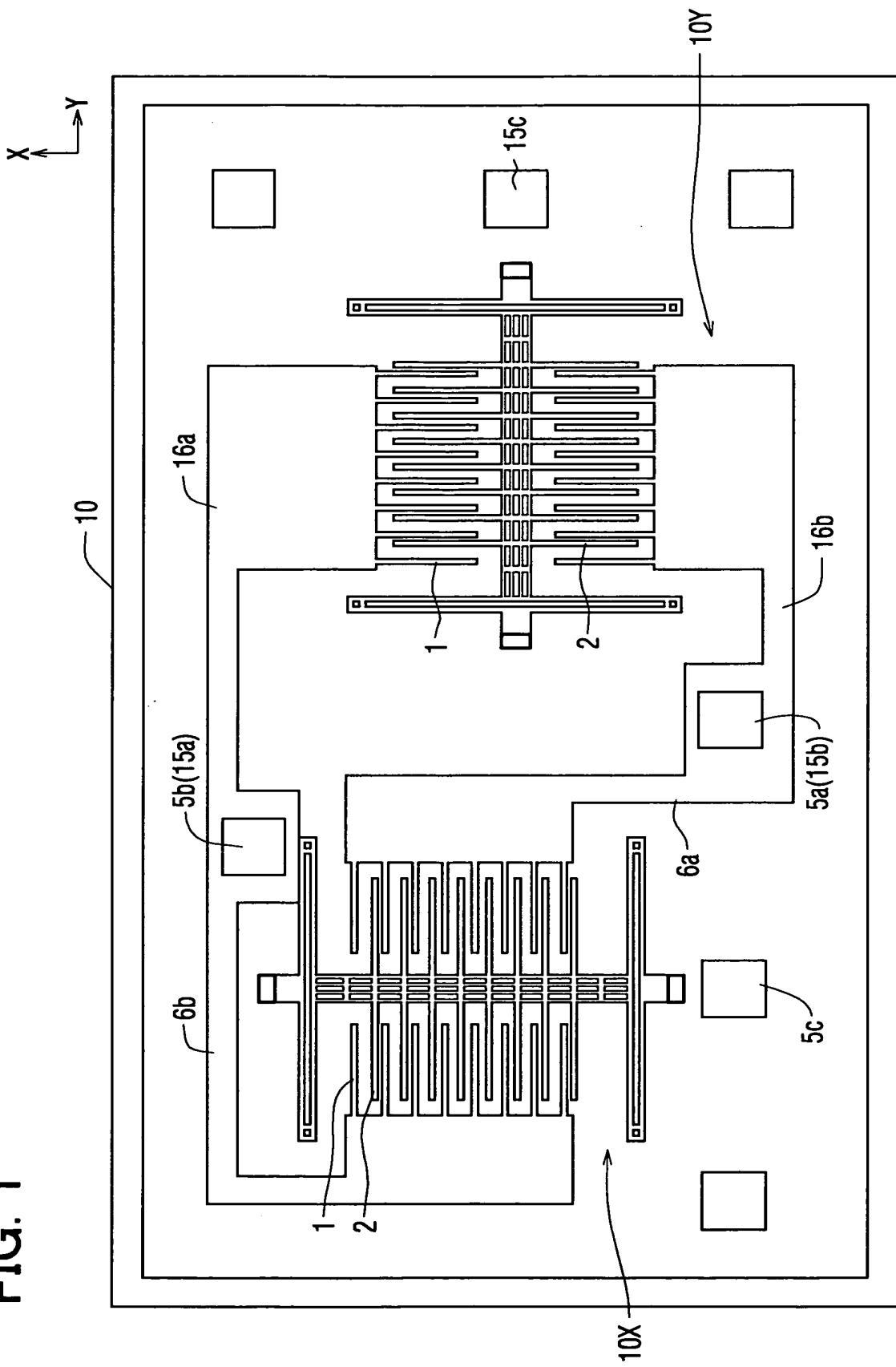


FIG. 2

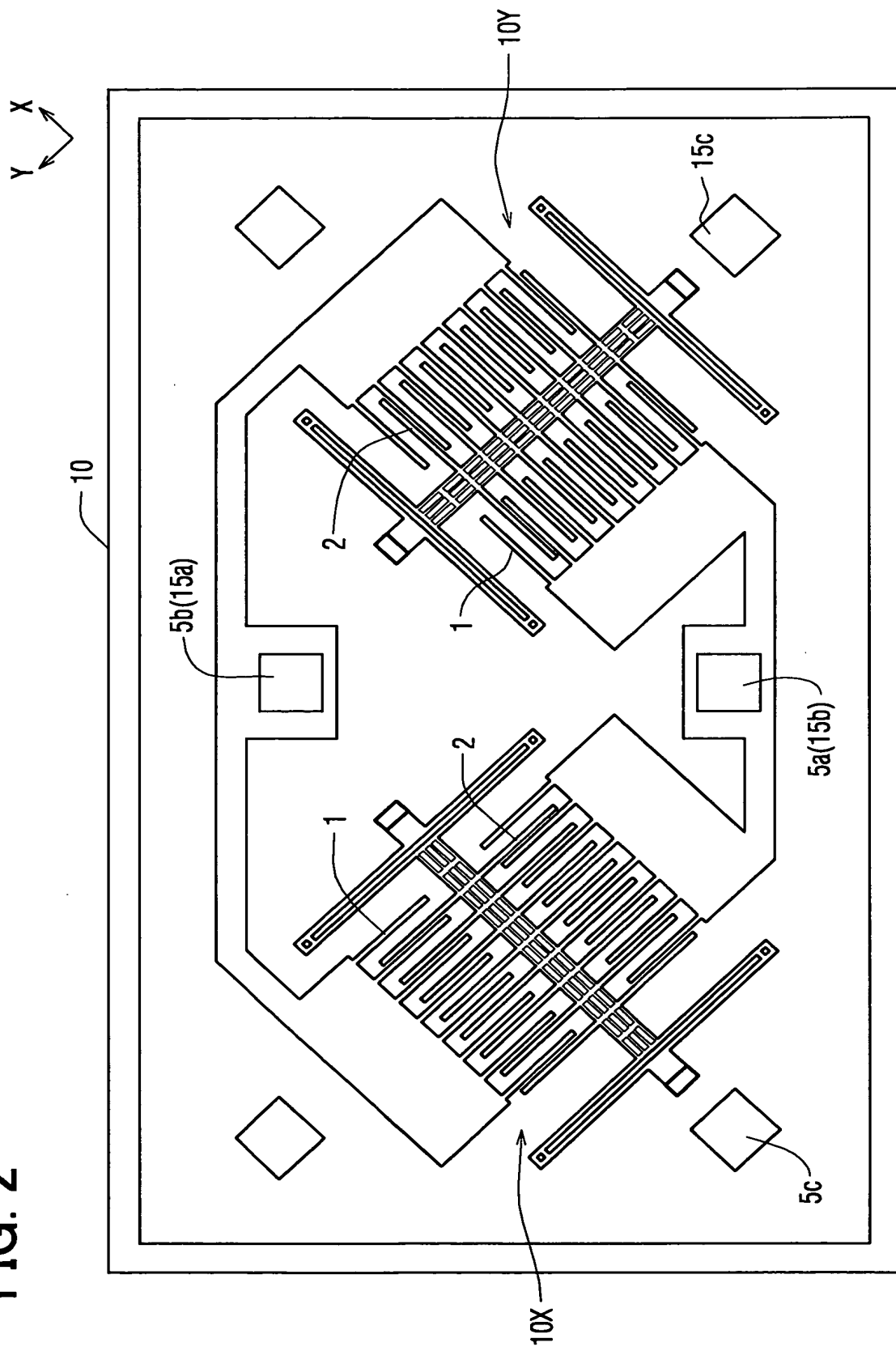


FIG. 3

FIG. 3 is a schematic diagram of a semiconductor device layout. The layout is enclosed in a rectangular frame labeled 10. A central region, labeled 10X and 10X', contains a complex pattern of horizontal and vertical lines, with labels 1 and 2 pointing to specific features. To the right of this central region, there are four square blocks labeled 5b, 5a(15b), 5c, and 15c. Above the central region, there are two square blocks labeled 15a and 15c. A coordinate system is shown in the top left corner with axes X, Y, and X'.

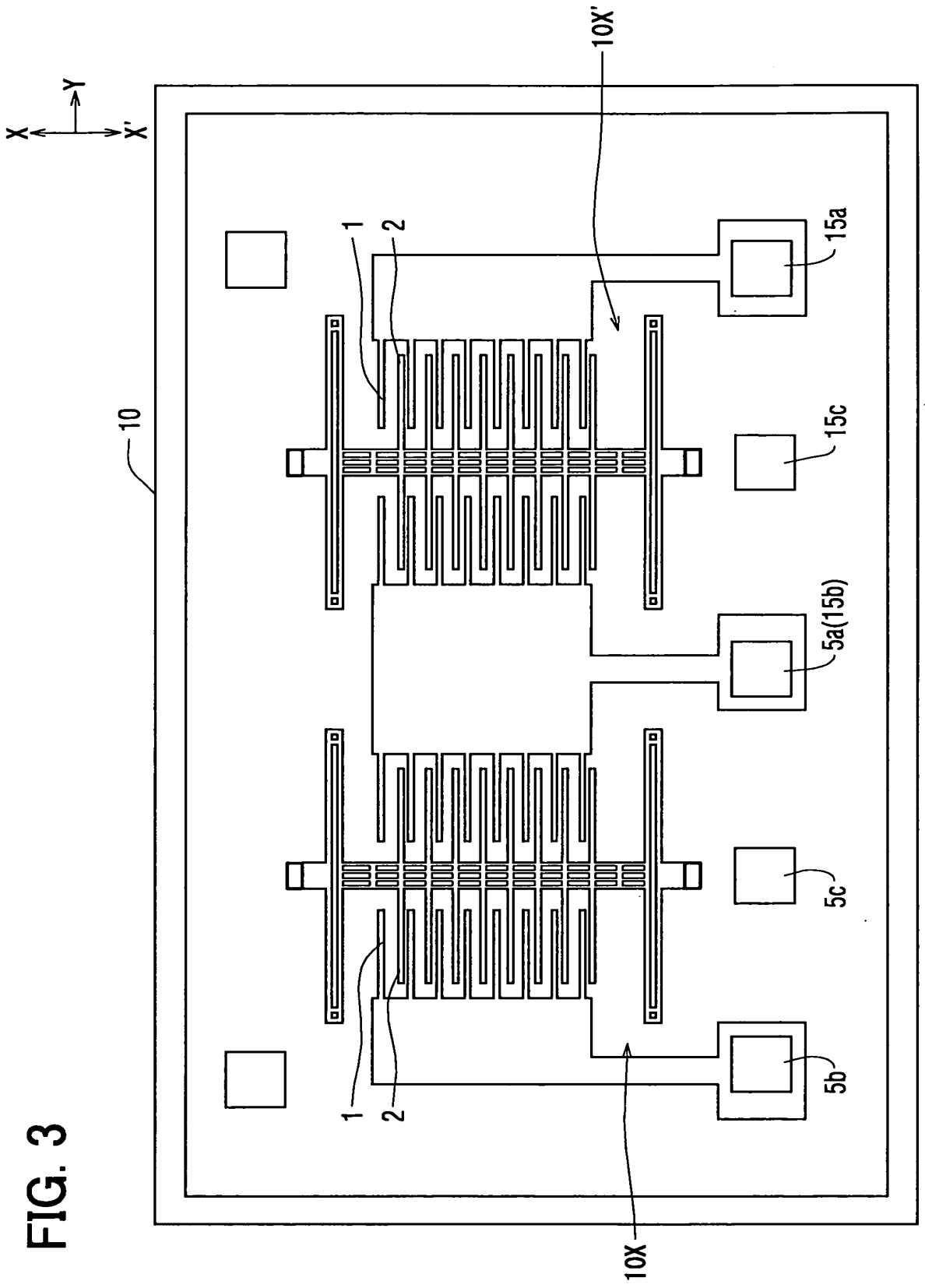


FIG. 4A
PRIOR ART

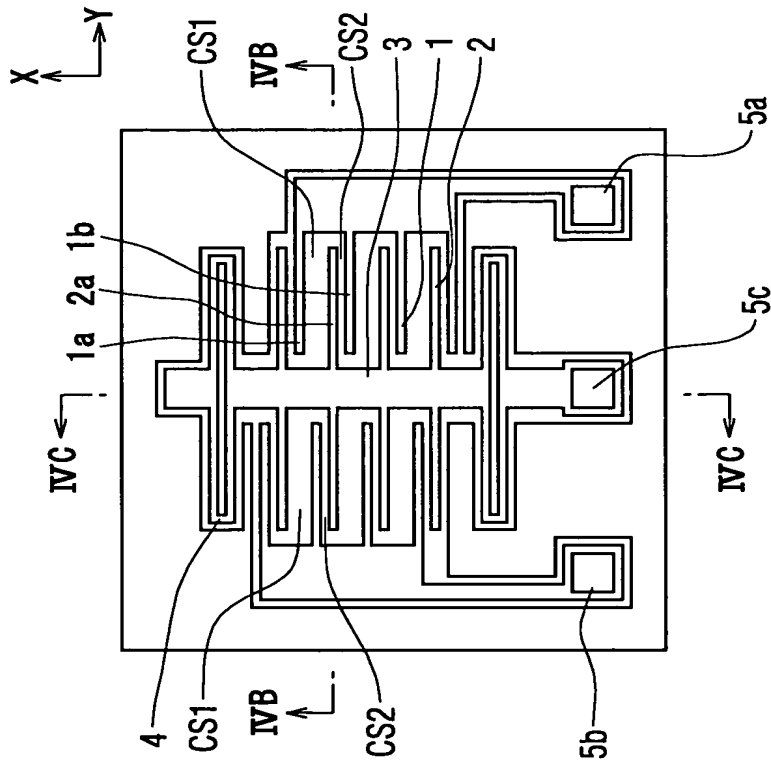


FIG. 4C
PRIOR ART

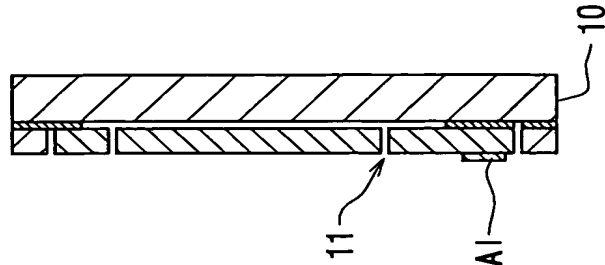


FIG. 4B
PRIOR ART

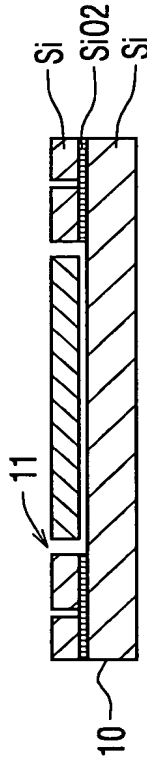


FIG. 5
PRIOR ART

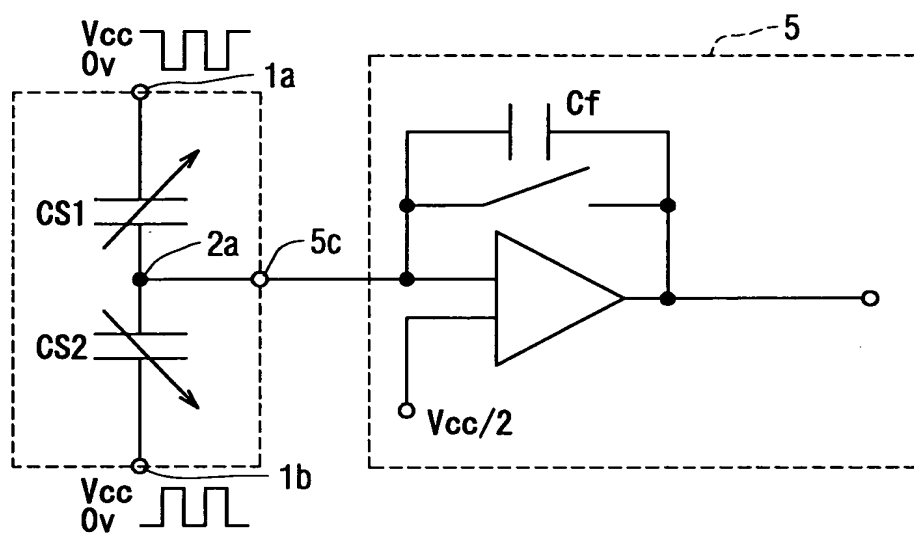


FIG. 6
PRIOR ART

